## REMARKS

Claims 1-12 are currently pending in the application. By this response, no claims are amended, added, or canceled. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

### *Allowable Subject Matter*

Applicants appreciate the indication that claims 4-6 contain allowable subject matter and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants submit that all of the claims are in condition for allowance for the following reasons.

### *Improper Final Rejection*

Applicants respectfully submit that the Office Action dated November 30, 2006, was improperly made final, and request withdrawal of the finality of the Office Action and issuance of a new non-final Office Action. MPEP §706.07(a) provides the following guidance on when a second office action may properly be made final:

> Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p).

Applicants submit that a new ground of rejection has been applied to claims 1-3, 7, and 10 that was not necessitated by an amendment to the claims. More specifically, claims 1-12 were previously rejected on the ground of non-statutory double patenting based upon *In re*

*Schneller*. Claims 1-3, 7, and 10 were not amended in the response dated September 1, 2006. However, in the Final Office Action dated November 30, 2006, the double patenting rejection based upon *In re Schneller* was withdrawn, and claims 1-3, 7, and 10 were rejected based upon the judicially created doctrine of obviousness-type double patenting. Because claims 1-3, 7, and 10 were not amended, the new double patenting rejection in the Final Office Action constitutes a new ground of rejection that was not necessitated by an amendment to the claims. Therefore, the Final Office Action was improperly made final.

Accordingly, Applicants respectfully request that the finality of the outstanding Office Action be withdrawn, and a new non-final Office Action be issued.

***Double Patenting Rejection***

Claims 1-3, 7, and 10 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-11 of U.S. Patent No. 6,877,048. This rejection is respectfully traversed.

Applicants submit herewith an executed Terminal Disclaimer pursuant to 37 C.F.R. 1.321(c). The enclosed Terminal Disclaimer is filed merely to remove any issue as to whether the claims of the above-identified application conflict in any way with those of U.S. Patent No. 6,877,048. Applicants emphasize that the Terminal Disclaimer is being filed only to expedite the allowance of the pending claims, and does not express any agreement or acquiescence with the rejection of record.

Accordingly, Applicants respectfully request that the double patenting rejection over claims 1-3, 7, and 10 be withdrawn.

***35 U.S.C. §102 Rejection***

Claims 1, 2 and 7-12 were rejected under 35 U.S.C. §102(e) for being anticipated by U.S. Patent No. 6,219,728 issued to Yin ("Yin"). This rejection is respectfully traversed.

To anticipate a claim, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference. See MPEP §2131. Applicants submit that Yin does not show each and every feature of the claimed invention.

The present invention generally relates to the field of dynamic memory allocation in a networking protocol handler, and, more particularly, to a method and apparatus for dynamically allocating memory between inbound and outbound paths of a protocol handler so as to optimize the ratio of a given amount of memory between the inbound and outbound memory buffers. Independent claim 1 recites, in pertinent part:

> ... an inbound memory for receiving data packets;
> an outbound memory for transmitting data packets; and
> circuitry capable of dynamically allocating memory from the inbound memory for use by the outbound memory or from the outbound memory for use by the inbound memory.

Independent claim 7 recites, in pertinent part:

> ... receiving data packets in an inbound memory buffer;
> transmitting data packets with an outbound memory buffer; and
> dynamically allocating memory from the inbound memory buffer for use by the outbound memory buffer or the outbound memory buffer for use by the inbound memory buffer.

Independent claim 10 recites, in pertinent part:

> ... means for receiving data packets in an inbound memory buffer;

> means for transmitting data packets with an outbound memory buffer; and
>
> means for dynamically allocating memory from the inbound memory buffer for use by the outbound memory buffer or the outbound memory buffer for use by the inbound memory buffer.

The Examiner asserts that element 106 shown in FIGS. 5-7 of Yin constitutes inbound memory buffers. The Examiner further asserts that elements 112-116 (address queues $Q_1 \ldots Q_n$) constitute outbound memory buffers. The Examiner further asserts that Yin discloses a processor in FIG. 8A that constitutes circuitry capable of dynamically allocating memory from the inbound memory for use by the outbound memory or from the outbound memory for use by the inbound memory. Applicants respectfully disagree.

Yin does not disclose an inbound memory for receiving data packets and an outbound memory for transmitting data packets, as recited in the claimed invention. Moreover, because Yin does not have separate inbound and outbound memory, it is impossible for Yin to have circuitry that dynamically allocates memory from the inbound memory for use by the outbound memory (or vice versa), as recited by the claimed invention. Therefore, Yin does not disclose each and every feature of independent claims 1, 7, and 10.

As previously discussed, Yin's invention is related to a system for allocating shared memory resources among various ports and discarding incoming or outgoing data cells as necessary. In describing FIG. 2 with respect to the invention, Yin shows a shared memory switch 100 comprising a shared memory 102 and multiple address queues 104. The shared memory 102 contains a plurality of memory buffers or locations that are shared by all of the address queues 104. That is, when a data cell is received by switch 100, the data cell is stored at any available buffer in the shared memory 102. The memory address is then added to the

appropriate address queue 104. When the cell is removed from the shared memory 102, the associated address is deleted from the address queue. Thus, it is seen that there is a single shared memory 102, and the address queues 104 contain memory addresses related to the buffer locations within the shared memory 102. The address queues 104 do not contain the actual cell data (column 4, lines 20-30).

In FIGS. 5-7, Yin shows examples of the memory switch 100 under different memory usage conditions. In FIG. 5A, shared memory 102 contains a plurality of data cells 106. The three address queues 112, 114, and 116 correspond to the address queues 104 described with respect to FIG. 2 (and are what the Examiner refers to as $Q_1 \ldots Q_n$). Address queues 114 and 116 (i.e., $Q_2$ and $Q_3$) are empty, indicating that the queues are currently inactive. Address queue 112 (i.e., $Q_1$) is active as indicated by a plurality of addresses 118 stored in the queue. Each address 118 stored in the address queue 112 (i.e., $Q_1$) indicates a memory address within shared memory 102 containing the actual data cell to be transmitted (see line 66 of col. 4 through line 10 of col. 5). Yin discloses a system and method for dynamically changing the threshold 122 (i.e., maximum available use) of each used address queue based upon the amount of free memory 110 remaining in the shared memory 102 (see FIGS. 6-7 and line 64 of col. 5 through line 15 of col. 6). In this manner, shortcomings associated with static thresholds can be overcome (see line 48 of col. 1 through line 19 of col. 2).

However, Yin does not disclose an inbound memory for receiving data packets and an outbound memory for transmitting data packets, as recited in the claimed invention. Yin only discloses a single shared memory 102 that is used for both input and output. The single shared memory 102 does not, however, constitute an inbound memory and an outbound memory. That is, an inbound data cell is stored in a buffer of the shared memory 102, and then later is discarded

from the same buffer in the shared memory 102. There is no separate inbound memory for receiving data packets and outbound memory for transmitting data packets, as recited in the claimed invention. Moreover, because Yin does not have separate inbound and outbound memory, it is impossible for Yin to have circuitry that dynamically allocates memory from the inbound memory for use by the outbound memory (or vice versa), as recited by the claimed invention. Therefore, Yin does not disclose each and every feature of independent claims 1, 7, and 10.

In fact, Yin discloses a system that Applicants are aware of and that implementations of the instant invention provide improvements over. Yin discloses that the system is based upon asynchronous transfer mode (ATM) handling of data cells and packets (col. 3, lines 55-65). Applicants are aware of ATM systems, as they are discussed in the Background section of the instant invention. Such systems use a single fixed amount of shared memory. In ATM systems, inbound data cells can be routed to any buffer in a pool of the single shared memory. From this same buffer, the data cell can be directly routed to the appropriate outbound path. Because ATM systems contain only a single shared memory, they do not comprise an inbound memory and an outbound memory and the capability to allocate memory from the inbound memory to the outbound memory (or vice versa).

Contrary to the Examiner's assertions, the address queues 112, 114, and 116 (i.e., $Q_1$, $Q_2$, and $Q_3$) of Yin do not constitute an outbound memory for transmitting data packets. Yin explicitly states that the address queues contain memory addresses related to cell buffer locations in the shared memory 102, and do not contain the actual cell data (col. 4, lines 23-25). The address queues do not provide the functionality of transmitting data packets. Therefore, the

queues (i.e., $Q_1$, $Q_2$, and $Q_3$) shown in FIGS. 5-7 do not constitute outbound memory for transmitting data packets, as recited in the claimed invention.

Even assuming *arguendo* that the shared memory 102 constitutes an inbound memory for receiving data packets and the address queues 112, 114, 116 (i.e., $Q_1$, $Q_2$, and $Q_3$) constitute an outbound memory for transmitting data packets, which Applicants do not concede, there is no mention whatsoever in Yin that memory from the shared memory 102 can be allocated for use by the address queues 112, 114, 116 (i.e., $Q_1$, $Q_2$, and $Q_3$), or vice versa. Contrary to the Examiner's assertion, there is no disclosure in Yin that a portion of shared memory 102 may be allocated for use by the address queues 112, 114, 116 (i.e., $Q_1$, $Q_2$, and $Q_3$). Physical portions of the shared memory 102 simply are not used by the address queues 112, 114, 116 (i.e., $Q_1$, $Q_2$, and $Q_3$). Therefore, Yin does not disclose circuitry that dynamically allocates memory from the inbound memory for use by the outbound memory (or vice versa), as recited by the claimed invention.

With further regard to dynamically allocating memory from the inbound memory for use by the outbound memory, Applicants respectfully submit that the Examiner is improperly interpreting the disclosure of Yin. The Examiner states "[w]hile the data cells and address queue may be occupied on the same monolithic piece of memory, they do not overlap..." and "element 110 shows the physical area of the shared memory, element 102, where the address queue occupies" (Final Office Action, page 3). Applicants respectfully disagree and submit that the address queues 112, 114, 116 do no reside in shared memory 102.

Contrary to the Examiner's assertions, the address queues 112, 114, 116 are physically different from the shared memory 102. Yin explicitly discloses that the shared memory 102 may be a random access memory (RAM) device or similar memory device containing a plurality of

memory buffers or memory locations (col. 3, lines 54-56). Yin further discloses that switch 100 includes a plurality of address queues 104, and that the address queues 104 may be first-in-first-out (FIFO) buffers or similar queueing devices (col. 3, line 64 through col. 4, line 1). And, as shown in FIG. 2, the shared memory 102 is physically separate from the address queues 104 on the memory switch 100. Thus, the address queues 112, 114, 116, which are illustrative examples of address queues 104, are physically different from the shared memory 102. Therefore, because the address queues 112, 114, 116 are separate from the shared memory 102, and because Yin makes no mention whatsoever of allocating memory from the shared memory 102 for use by the address queues 112, 114, 116 (or vice versa), Yin cannot arguably disclose circuitry that dynamically allocates memory from the inbound memory for use by the outbound memory (or vice versa), as recited by the claimed invention.

Applicants respectfully submit that claims 2, 8, 9, 11, and 12 depend from allowable independent claims, and are allowable based upon the allowability of the respective independent claims.

Accordingly, Applicants respectfully request that the rejection over claims 1, 2 and 7-12 be withdrawn.

## CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
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